Zero-Drift, Single-Supply, Sensor Signal Amplifier with Digitally Programmable Gain and Offset

ANALOG DEVICES

Preliminary Technical Data AD8555

FEATURES

Very low offset voltage: 10uV max over temperature
Very low input offset voltage drift: 50nV/°C max
High CMRR: 96dB
Digitally programmable gain (span) and output offset voltage
Open and short wire fault detection
Low pass filtering
Externally programmable output clamp voltage for driving low-voltage ADCs
Very wide input and output ranges
Single supply operation from 2.7V to 5.5V supplies

APPLICATIONS

Brake pressure sensing
Manifold pressure sensing
Leak-down pressure detection
Fuel pressure sensing
Balanced bridge sensors
Precision current sensing

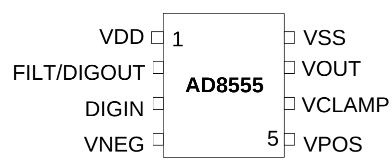
PRODUCT OVERVIEW

AD8555 is a zero-drift bridge sensor signal amplifier with digitally programmable gain and output offset. Designed to easily and accurately convert variable pressure sensor and strain bridge outputs to a well-defined output voltage range, AD8555 will also accurately amplify many other differential or single ended sensor outputs. AD8555 utilizes ADI's patented low noise auto-zero and DigiTrim® technologies to create an incredibly accurate and flexible signal processing solution in a very compact footprint. In addition to extremely low input offset voltage and input offset voltage drift and very high DC and AC CMRR, the AD8555 also includes a pull-up current source at each analog input to allow open wire and shorted wire fault detection, and a low-pass filter function implemented via a single low-cost external capacitor. Output clamping set via an external reference voltage allows the AD8555 to drive lower voltage ADCs safely and accurately.

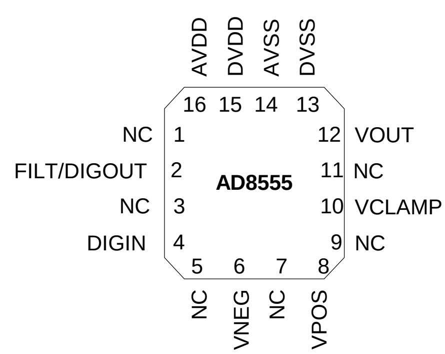
Gain is digitally programmable in a wide range from 70 to 1280 through a serial data interface. Gain adjustment can be fully simulated in-circuit and then permanently programmed with proven and reliable poly-fuse technology. Output offset voltage is also digitally programmable and is ratiometric to the supply voltage. When used in conjunction with an ADC referenced to the same supply, the system accuracy becomes immune to normal supply voltage variations. Output offset voltage can be adjusted with a resolution of better than 0.4% of the difference between VDD and VSS. A lockout trim after gain and offset adjustment further assures field reliability.

AD8555AR is fully specified over the extended industrial (automotive) temperature range from –40°C to +125°C. Operating from single-supply voltages from 2.7V to 5.5V, the AD8555 is offered in the narrow 8-lead SOIC package and the 4 x 4mm 16-lead LFCSP.

8-Lead SOIC
(R-8 Suffix)



16-Lead LFCSP
(CP-16 Suffix)



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ELECTRICAL SPECIFICATIONS

(@ V_{DD}=+5.0V, V_{SS}=0.0V V_{CM} = +2.5V, V_O=+2.5V, -40°C ≤ T_A ≤ +125°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SYSTEM PERFORMANCE						
Input Offset Voltage	V_{OS}			3	10	μV
Input Bias Current @ VPOS, VNEG	I_B	T_A = 25°C	8	18	28	nA
					30	nA
Input Bias Current @VCLAMP		T_A = 25°C		10		pA
					5	nA
Input Offset Current @ VPOS, VNEG	I_{OS}	T_A = 25°C		1	5	nA
					8	nA
Input Voltage Range @ VPOS, VNEG			0.9		3.6	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 3.9V, A_V=70	70			dB
		V_{CM} = 0V to 3.9V, A_V=1280	96			dB
Input Referred Noise		T_A = 25°C		32		nV/√Hz
Ratiometricity				50		ppm
Linearity				20		ppm
Differential Gain Accuracy				1	3	%
Differential Gain Temperature Coeff.					20	ppm/°C
DAC Accuracy				1	3	%
DAC Offset				5	50	mV
DAC Temperature Coefficient					200	ppm/°C
RF			9.6	16	22.4	kΩ
RF Temperature Coefficient				700		ppm/°C
VCLAMP Input Range			1.8		5	V
VD1			0.6	1.1	1.5	V
RP			100			kΩ
POWER SUPPLY						
Supply Current	I_{SY}	V_O = 2.5V			4	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	1st gain stage, T_A = 25°C		2		MHz
		2nd gain stage, T_A = 25°C		8		MHz
AMPLIFIER PERFORMANCE						
Amplifiers A1, A2, A3						
INPUT CHARACTERISTICS						
Offset Voltage				3	10	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.01	0.05	μV/°C
Input Bias Current		T_A = 25°C		30	100	pA
Input Offset Current		T_A = 25°C		50	200	pA
Input Voltage Range			0.5		3.9	V
DYNAMIC PERFORMANCE						
Gain Bandwidth Product						
Amplifiers A1, A2	GBP	T_A = 25°C		2		MHz
Amplifier A3		T_A = 25°C		8		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1kHz, T_A = 25°C		25		nV/√Hz

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
INPUT CHARACTERISTICS						
DIGIN pulse width to load 0	tw0	T_A = 25°C	0.05		10	µs
DIGIN pulse width to load 1	tw1	T_A = 25°C	50			µs
time between pulses at DIGIN	tws	T_A = 25°C	10			µs
DIGIN low		T_A = 25°C	0		1	V
DIGIN high		T_A = 25°C	4		5	V
DIGOUT logic 0		T_A = 25°C	0		1	V
DIGOUT logic 1		T_A = 25°C	4		5	V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ....+6V
Input Voltage .... VSS –0.3V to VDD + 0.3V
Differential Input Voltage[1] ....±5.0V
Output Short-Circuit Duration to VSS or VDD…………Indefinite
Storage Temperature Range……………………..-65°C to +150°C
Operating Temperature Range…………………..…..40°C to +125°C
Junction Temperature Range…………………....-65°C to +150°C
Lead Temperature Range (Soldering, 10 sec).……………+300°C

Package Type	JA[2]	JC	Units
8-Lead SOIC (R)	158	43	°C/W
16-Lead LFCSP (CP)	44	31.5	°C/W

NOTES

[1] Differential input voltage is limited to ±5.0 volts or ± the supply voltage, whichever is less.

[2] JA is specified for the worst case conditions, i.e. JA is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

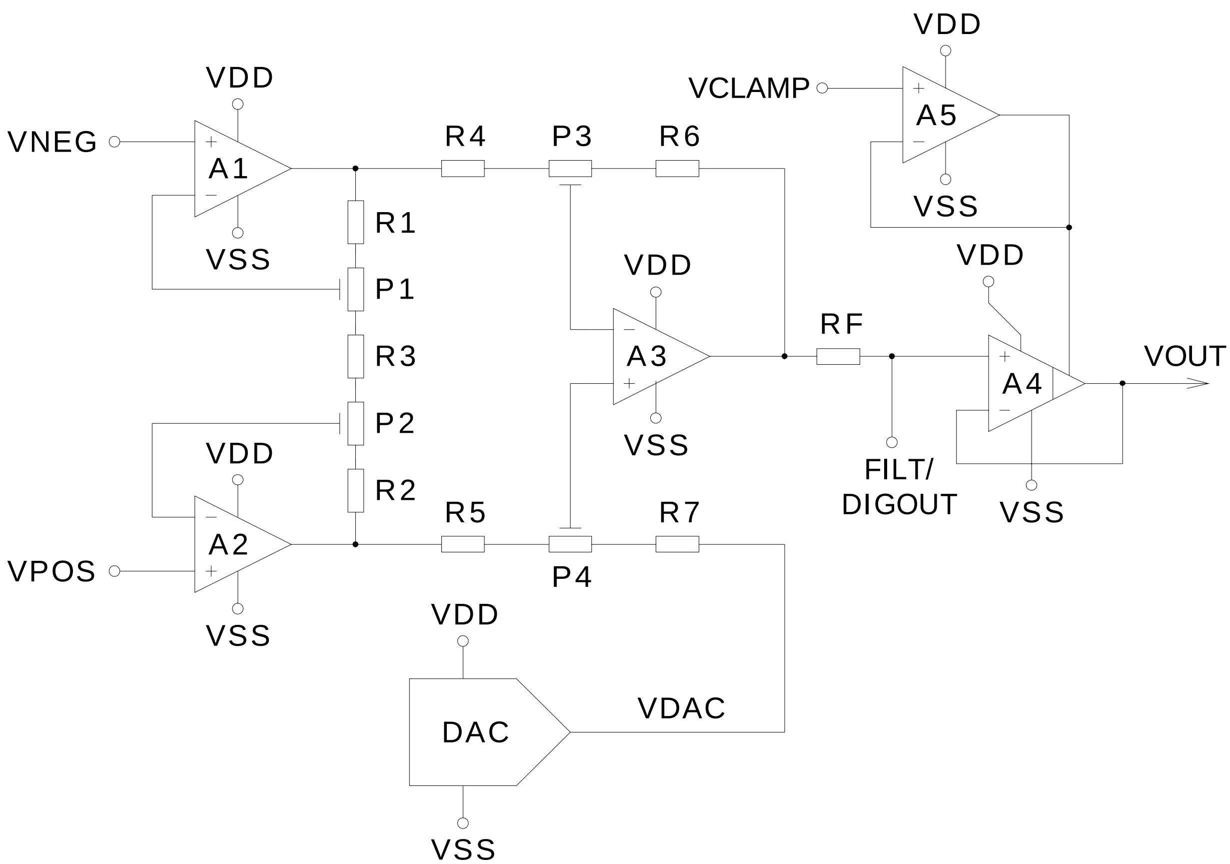
Model	Temperature Range	Package Description	Package Option
AD8555AR	-40°C to +125°C	8-Lead SOIC	SO-8
AD8555ACP	-40°C to +125°C	16-Lead LFCSP	CP-16

PIN FUNCTION DESCRIPTIONS

SOIC / LFCSP	Name	Function
Pin 1 / Pins 15, 16	V_{DD} / DV_{DD},AV_{DD}	Positive supply voltage
Pin 2 / Pin 2	FILT/DIGOUT	Unbuffered amplifier output in series with a resistor RF. Adding a capacitor between FILT and VDD or VSS will implement a low-pass filtering function. In read mode, this pin functions as a digital output
Pin 3 / Pin 4	DIGIN	Digital input
Pin 4 / Pin 6	VNEG	Negative amplifier input (inverting input)
Pin 5 / Pin 8	VPOS	Positive amplifier input (non-inverting input)
Pin 6 / Pin 10	VCLAMP	Set clamp voltage at output
Pin 7 / Pin 12	VOUT	Buffered amplifier output -- buffered version of the signal at the FILT/DIGOUT pin. In read mode, VOUT is a buffered digital output.
Pin 8 / Pins 13, 14	V_{SS} / $DV_{SS,}$ AV_{SS}	Negative supply voltage

Theory of Operation

AD8555 Functional Schematic



A1, A2, R1, R2, R3, P1 and P2 form the first gain stage of the differential amplifier. A1 and A2 are auto-zeroed op-amps to minimize input offset errors. P1 and P2 are digital potentiometers, guaranteed to be monotonic. Programming of P1 and P2 allow the first stage gain to be varied from 4.0 to 6.4 with 7-bit resolution (see Table 1 and equation (3)), giving a fine gain adjustment resolution of 0.37%. R1, R2, R3, P1 and P2 each have a similar temperature coefficient, so the first stage gain temperature coefficient is lower than 200ppm/°C.

A3, R4, R5, R6, R7, P3 and P4 form the second gain stage of the differential amplifier. A3 is also an auto-zeroed op-amp to minimize input offset errors. P3 and P4 are digital potentiometers, allowing the second stage gain to be varied from 17.5 to 200 in 8 steps (see Table 2); they allow the gain to be varied over a wide range. R4, R5, R6, R7, P3 and P4 each have a similar temperature coefficient, so the second stage gain temperature coefficient is lower than 200ppm/°C.

RF together with an external capacitor connected between FILT/DIGOUT and VSS or VDD form a low pass filter. The filtered signal is buffered by A4 to give a low impedance output at VOUT. RF is nominally 16kΩ, allowing a 1kHz low pass filter to be implemented by connecting a 10nF external capacitor between FILT/DIGOUT and VSS or between FILT/DIGOUT and VDD. If low-pass filtering is not needed then the FILT/DIGOUT pin must be left floating.

A5 implements a voltage buffer which provides the positive supply to the amplifier output buffer A4. Its function is to limit VOUT to a maximum value, useful for driving analog-to-digital converters operating on supply voltages lower than VDD. The input to A5, VCLAMP, has a very high input resistance. It should be connected to a known voltage and not left floating. However, the high input impedance allows the clamp voltage to be set using high impedance source, e.g. a potential divider. If the maximum value of VOUT does not need to be limited, VCLAMP should be connected to VDD.

A4 implements a rail-to-rail input and output unity-gain voltage buffer. The output stage of A4 is supplied from a buffered version of VCLAMP instead of VDD, allowing the positive swing to be limited. The maximum output current is limited between 5mA to 10mA.

An 8-bit digital-to-analog converter (DAC) is used to generate a variable offset for the amplifier output. This DAC is guaranteed to be monotonic. To preserve the ratiometric nature of the input signal, the DAC references are driven from VSS and VDD, and the DAC output can swing from VSS (code 0) to VDD (code 255). The 8-bit resolution is equivalent to 0.39% of the difference between VDD and VSS (e.g. 19.5mV with a 5V supply). The DAC output voltage (VDAC) is given approximately by equation (1) below:

$$VDAC \approx \left(\frac{code + 0.5}{256}\right)(VDD - VSS) + VSS \qquad (1)$$

The temperature coefficient of VDAC is lower than 200ppm/°C.

The amplifier output voltage (VOUT) is given by equation (2) below:

$$VOUT = GAIN(VPOS - VNEG) + VDAC \qquad (2)$$

where GAIN is the product of the first and second stage gains.

Gain values

Table 1: First Stage Gain vs. Gain Code

First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain	First Stage Gain Code	First Stage Gain
0	4.000	32	4.503	64	5.069	96	5.706
1	4.015	33	4.520	65	5.088	97	5.727
2	4.030	34	4.536	66	5.107	98	5.749
3	4.045	35	4.553	67	5.126	99	5.770
4	4.060	36	4.570	68	5.145	100	5.791
5	4.075	37	4.587	69	5.164	101	5.813
6	4.090	38	4.604	70	5.183	102	5.834
7	4.105	39	4.621	71	5.202	103	5.856
8	4.120	40	4.638	72	5.221	104	5.878
9	4.135	41	4.655	73	5.241	105	5.900
10	4.151	42	4.673	74	5.260	106	5.921
11	4.166	43	4.690	75	5.280	107	5.943
12	4.182	44	4.707	76	5.299	108	5.965
13	4.197	45	4.725	77	5.319	109	5.988
14	4.213	46	4.742	78	5.339	110	6.010
15	4.228	47	4.760	79	5.358	111	6.032
16	4.244	48	4.778	80	5.378	112	6.054
17	4.260	49	4.795	81	5.398	113	6.077
18	4.276	50	4.813	82	5.418	114	6.099
19	4.291	51	4.831	83	5.438	115	6.122
20	4.307	52	4.849	84	5.458	116	6.145
21	4.323	53	4.867	85	5.479	117	6.167
22	4.339	54	4.885	86	5.499	118	6.190
23	4.355	55	4.903	87	5.519	119	6.213
24	4.372	56	4.921	88	5.540	120	6.236
25	4.388	57	4.939	89	5.560	121	6.259
26	4.404	58	4.958	90	5.581	122	6.283
27	4.420	59	4.976	91	5.602	123	6.306
28	4.437	60	4.995	92	5.622	124	6.329
29	4.453	61	5.013	93	5.643	125	6.353
30	4.470	62	5.032	94	5.664	126	6.376
31	4.486	63	5.050	95	5.685	127	6.400

$$GAIN1 \approx 4 * \left(\frac{6.4}{4}\right)^{\left(\frac{code}{127}\right)} \quad (3)$$

Table 2: Second Stage Gain and Gain Ranges vs. Gain Code

Second Stage Gain Code	Second Stage Gain	Minimum Combined Gain	Maximum Combined Gain
0	17.5	70	112
1	25	100	160
2	35	140	224
3	50	200	320
4	70	280	448
5	100	400	640
6	140	560	896
7	200	800	1280

Open Wire Fault Detection

The inputs to A1 and A2, VNEG and VPOS, each have a comparator to detect whether VNEG or VPOS exceed a threshold voltage, nominally VDD-1.1V. If (VNEG > VDD-1.1V) OR (VPOS > VDD-1.1V), then VOUT is clamped to VSS. The output current limit circuit is disabled in this mode, but the maximum sink current is approximately 50mA when VDD=5V. The inputs to A1 and A2, VNEG and VPOS, are also pulled up to VDD by currents IP1 and IP2. These are nominally 18nA each, and matched to within 5nA. If the inputs to A1 or A2 are accidentally left floating (e.g. an open wire fault), then IP1 and IP2 will pull them to VDD, which would cause VOUT to swing to VSS, allowing this fault to be detected. It is not possible to disable IP1 and IP2, nor the clamping of VOUT to VSS when VNEG or VPOS approach VDD.

Shorted Wire Fault Detection

The AD8555 provides fault detection, in the case where VPOS, VNEG, and VCLAMP shorts to VDD and VSS. Figure 1 shows the voltage regions at VPOS, VNEG, and VCLAMP which trigger an error condition. When an error condition occurs, the VOUT pin is shorted to VSS. Table 3 lists the voltage levels shown in Figure 1.

Figure 1: Voltage Regions at VPOS, VNEG, and VCLAMP, Which Trigger a Fault Condition

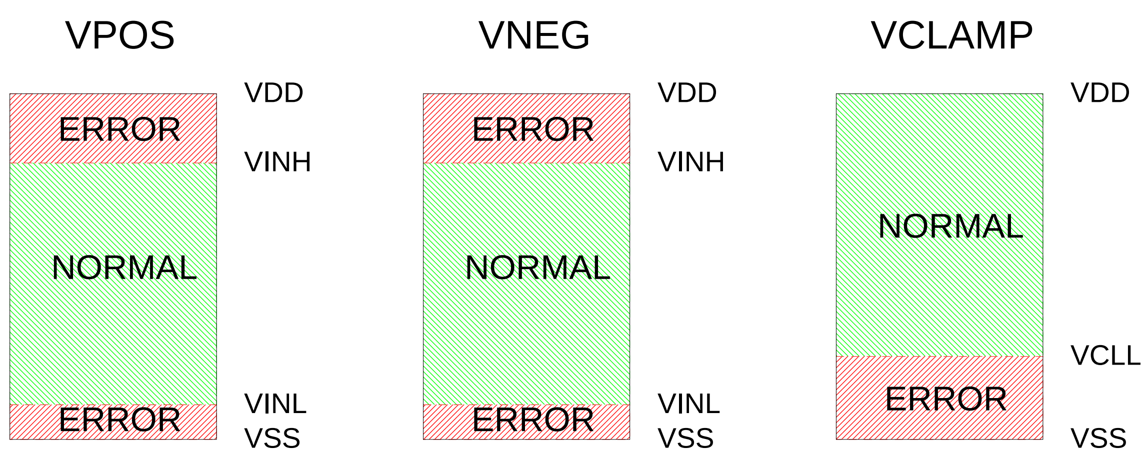


Table 3: Definition of VINL, VINH and VCLL

Voltage	Minimum Value	Maximum Value	Purpose
VINH	VDD – 1.3V	VDD – 0.7V	Short to VDD Fault Detection
VINL	0.05 * VINH	0.15 * VINH	Short to VSS Fault Detection
VCLL	VSS + 1.0V	VSS + 1.7V	Short to VSS Fault Detection

Floating VPOS, VNEG, or VCLAMP fault detection

A floating fault condition at the VPOS, VNEG, or VCLAMP pins is detected by using a low current to pull a floating input into an error voltage range defined in the previous section. In this way, the VOUT pin is shorted to VSS when a floating input is detected. Table 4 lists the currents used.

Table 4: Floating Fault Detection at VPOS, VNEG, and VCLAMP

Pin	Current	Goal of Current
VPOS	12nA to 24nA pull-up	Pull VPOS above VINH
VNEG	12nA to 24nA pull-up	Pull VNEG above VINH
VCLAMP	0.3µA to 2µA pull-down	Pull VCLAMP below VCLL

Device Programming

Digital Interface

The digital interface allows the first stage gain, second stage gain, and output offset to be adjusted and allows desired values for these parameters to be permanently stored by selectively blowing polysilicon fuses. To minimize pin count and board space, a single-wire digital interface is used. The digital input pin, DIGIN, has hysteresis to minimize the possibility of inadvertent triggering with slow signals. It also has a pull-down current sink to allow it to be left floating when programming is not being performed. The pull-down insures inactive status of the digital input by forcing a DC low voltage on DIGIN.

A short pulse at DIGIN from low to high and back to low again (e.g. between 50ns and 10µs long) loads a 0 into a shift register. A long pulse at DIGIN (e.g. 50µs or longer) loads a 1 into the shift register. The time between pulses should be at least 10µs. Assuming VSS=0V, voltages at DIGIN between VSS and 0.2*VDD are recognized as a low, and voltages at DIGIN between 0.8*VDD and VDD are recognized as a high. A timing diagram example showing the waveform for entering code 010011 into the shift register is shown in Figure 2.

Figure 2: Timing diagram for code 010011

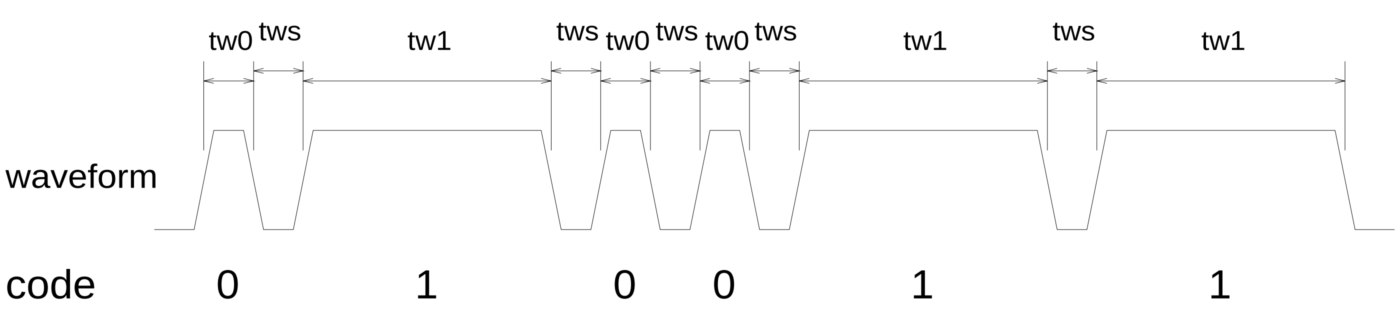


Table 5: Timing Specifications

Timing Parameter	Description	Specification
tw0	pulse width for loading 0 into shift register	between 50ns and 10µs
tw1	pulse width for loading 1 into shift register	>= 50µs
tws	width between pulses	>= 10µs

A 38-bit serial word is used, divided into 6 fields. Assuming each bit can be loaded in 60µs, the 38-bit serial word to be transferred in 2.3ms. Table 6 summarizes the word format.

Table 6: 38-bit serial word format

field 0	bits 0 to 11	12-bit start of packet "1000 0000 0001"
field 1	bits 12 to 13	2-bit function 00: change sense current 01: simulate parameter value 10: program parameter value 11: read parameter value
field 2	bits 14 to 15	2-bit parameter 00: second stage gain code 01: first stage gain code 10: output offset code 11: other functions
field 3	bits 16 to 17	2-bit dummy "10"
field 4	bits 18 to 25	8-bit value parameter 00 (second stage gain code):3 LSBs used parameter 01 (first stage gain code): 7 LSBs used parameter 10 (output offset code): all 8 bits used parameter 11 (other functions): bit 0 (LSB): master fuse bit 1: fuse for production test at Analog Devices
field 5	bits 26 to 37	12-bit end of packet "0111 1111 1110"

Fields 0 and 5 are the "start of packet" and "end of packet" fields respectively. Matching the "start of packet" field with "1000 0000 0001" and the "end of packet" field with "0111 1111 1110" ensure that the serial word is valid and enables decoding of the other fields. Field 3 breaks up the data and ensures that no data combination can inadvertently trigger the "start of packet" and "end of packet" fields. Field 0 should be written first and field 5 written last. Within each field, the MSB must be written first and the LSB written last. The shift register features power-on-reset to minimize the risk of inadvertent programming; power-on-reset occurs when VDD is between 0.7V and 2.2V.

Initial State

Initially, all the polysilicon fuses will be intact. Each parameter will have the value 0 assigned. See Table 7 below.

Table 7: Initial state before programming

Second Stage Gain Code = 0	Second Stage Gain = 17.5
First Stage Gain Code = 0	First Stage Gain = 4.0
Output Offset Code = 0	Output Offset = VSS
Master Fuse = 0	Master Fuse Not Blown

When power is applied to a device, parameter values are taken either from internal registers if the master fuse is not blown, or from the polysilicon fuses if the master fuse is blown. Programmed values have no effect until the master fuse is blown. The internal registers feature power-on-reset so that unprogrammed devices enter a known state after power-up; power-on-reset occurs when VDD is between 0.7V and 2.2V.

Simulation Mode

The simulation mode allows any parameter to be changed temporarily. These changes are retained until the simulated value is reprogrammed, the power is removed or until the master fuse is blown. Parameters are simulated by setting field 1 to 01, selecting the desired parameter in field 2, and the desired value for the parameter in field 4. Note that a value of 11 for field 2 is ignored during the simulation mode. Examples of temporary settings are given below.

Set the second stage gain code (parameter 00) to 011 and hence the second stage gain to 50:
1000 0000 0001 01 00 10 0000 0011 0111 1111 1110

Set the first stage gain code (parameter 01) to 000 1011 and hence the first stage gain to 4.166.
1000 0000 0001 01 01 10 0000 1011 0111 1111 1110

A first stage gain of 4.166 together with a second stage gain of 50 gives a total gain of 208.3. This gain will have a maximum tolerance of 3%.

Set the output offset code (parameter 10) to 0100 0000 and hence the output offset to 1.260V when VDD=5V and VSS=0V. This output offset will have a maximum tolerance of 3%.
1000 0000 0001 01 10 10 0100 0000 0111 1111 1110

Programming Mode

Intact fuses give a bit value of 0. Bits with a desired value of 1 need to have the associated fuse blown. Since a relatively large current is needed to blow a fuse, only one fuse can be reliably blown at a time. Thus, a given parameter value may need several 38-bit words to allow reliable programming. A 5.5V supply is required when blowing fuses to minimize the ON resistance of the internal MOS switches which blow the fuse. The power supply must be able to deliver 250mA of current, and at least 0.1μF of decoupling capacitance is needed across the power pins of the device. A minimum period of 1ms should be allowed for each fuse to blow. There is no need to measure the supply current during programming - the best way to verify correct programming is to use the read mode to read back the programmed values, and to re-measure the gain and offset to verify these values. Programmed fuses have no effect on the gain and output offset until the master fuse is blown; after blowing the master fuse, the gain and output offset are determined solely by the blown fuses and the simulation mode is permanently deactivated.

Parameters are programmed by setting field 1 to 10, selecting the desired parameter in field 2, and a single bit with the value 1 in field 4.

As an example, suppose the user wished to set the second stage gain permanently to 50. Parameter 00 needs to have the value 0000 0011 assigned. Two bits have the value 1, so two fuses need to be blown. Since only one fuse can be blown at a time, the code
1000 0000 0001 10 00 10 0000 0010 0111 1111 1110
can be used to blow one fuse. The MOS switch which blows the fuse closes when the complete packet is recognized, and opens when the start-of-packet, dummy, or end-of-packet fields are no longer valid. After 1ms, the second code

1000 0000 0001 10 00 10 0000 0001 0111 1111 1110
can be entered to blow the second fuse.

To set the first stage gain permanently to a nominal value of 4.151, parameter 01 needs to have the value 000 1011 assigned. Three fuses need to be blown; the following codes can be used, with a 1ms delay after each code:
1000 0000 0001 10 01 10 0000 1000 0111 1111 1110
1000 0000 0001 10 01 10 0000 0010 0111 1111 1110
1000 0000 0001 10 01 10 0000 0001 0111 1111 1110

To set the output offset permanently to a nominal value of 1.260V when VDD=5V and VSS=0V, parameter 10 needs to have the value 0100 0000 assigned. One fuse needs to be blown, and the following code can be used:
1000 0000 0001 10 10 10 0100 0000 0111 1111 1110

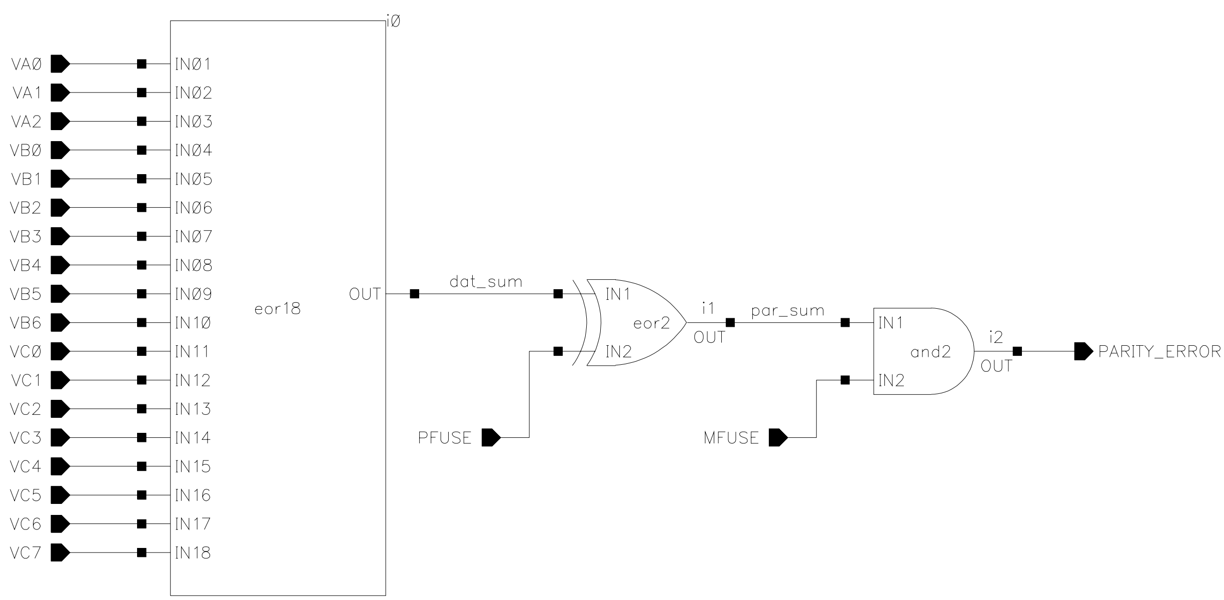
Finally, to blow the master fuse to deactivate simulation mode and prevent further programming, the code
1000 0000 0001 10 11 10 0000 0001 0111 1111 1110
can be used.

There are a total of 20 fuses. Since each fuse requires 1 ms to blow and each serial word can be loaded in 2.3 ms, the maximum time needed to program the fuses can be as low as 66 ms.

Parity Error Detection

A parity check is used to determine whether the programmed data of an AD8555 is valid, or whether data corruption has occurred in the non-volatile memory. Figure 3 shows the schematic implemented in the AD8555.

Figure 3: Functional circuit of AD8555 parity check



VA0 to VA2 is the 3-bit control signal for the second stage gain, VB0 to VB6 is the 7-bit control signal for the first stage gain, and VC0 to VC7 is the 8-bit control signal for the output offset. PFUSE is the signal from the parity fuse, and MFUSE is the signal from the master fuse.

The function of the 2-input AND gate (cell and2) is to ignore the output of the parity circuit (signal par_sum) when the master fuse has not been blown. PARITY_ERROR is set to 0 when MFUSE = 0. In the simulation mode, for example, parity check is disabled. After the master fuse has been blown, i.e. after the AD8555 has been programmed, the output from the parity circuit (signal par_sum) is fed to PARITY_ERROR. When PARITY_ERROR is 0, the AD8555 behaves as a programmed amplifier. When PARITY_ERROR is 1, a parity error has been detected, and VOUT is connected to VSS.

The 18-bit data signal (VA0 to VA2, VB0 to VB6, and VC0 to VC7) is fed to an 18-input exclusive-OR gate (cell eor18). The output of cell eor18 is the signal dat_sum. Dat_sum = 0 if there is an even number of 1's in the 18-bit word; dat_sum = 1 if there is an odd number of 1's in the 18-bit word. Examples are given in Table 8.

Table 8: Examples of dat_sum

Second Stage Gain Code	First Stage Gain Code	Output Offset Code	Number of Bits with 1	dat_sum
000	000 0000	0000 0000	0	0
000	000 0000	1000 0000	1	1
000	000 0000	1000 0001	2	0
000	000 0001	0000 0000	1	1
000	100 0001	0000 0000	2	0
001	000 0000	0000 0000	1	1
001	000 0001	1000 0000	3	1
111	111 1111	1111 1111	18	0

After the second stage gain, first stage gain, and output offset have been programmed, dat_sum should be computed and the parity bit should be set equal to dat_sum. If dat_sum is 0, the parity fuse **should not** be blown in order for the PFUSE signal to be 0. If dat_sum is 1, the parity fuse should be blown to set the PFUSE signal to 1. The code to blow the parity fuse is:

1000 0000 0001 10 11 10 0000 0100 0111 1111 1110

After the setting the parity bit, the master fuse can be blown to prevent further programming, using the code:

1000 0000 0001 10 11 10 0000 0001 0111 1111 1110

Signal par_sum is the output of the 2-input exclusive-OR gate (cell eor2). After the master fuse has been blown, PARITY_ERROR is set to par_sum. As mentioned earlier, the AD8555 behaves as a programmed amplifier when PARITY_ERROR = 0 (no parity error). On the other hand, VOUT is connected to VSS when a parity error has been detected (i.e. when PARITY_ERROR = 1).

Read Mode

The values stored by the polysilicon fuses can be sent to the FILT/DIGOUT pin to verify correct programming. Normally, the FILT/DIGOUT pin is connected only to the second gain stage output via RF. During read mode, however, the FILT/DIGOUT pin is also connected to the output of a shift register to allow the polysilicon fuse contents to be read. Since VOUT is a buffered version of FILT/DIGOUT, VOUT will also output a digital signal during read mode.

Read mode is entered by setting field 1 to 11 and selecting the desired parameter in field 2; field 4 is ignored. The parameter value, stored in the polysilicon fuses, is loaded into an internal shift register, and the MSB of the shift register is connected to the FILT/DIGOUT pin. Pulses at DIGIN shift the shift register contents out to the FILT/DIGOUT pin, allowing the 8-bit parameter value to be read after seven additional pulses; shifting occurs on the falling edge of DIGIN. An eighth pulse at DIGIN disconnects FILT/DIGOUT from the shift register and terminates the read mode. If a parameter value is less than 8 bits long, the MSBs of the shift register are padded with 0s.

For example, to read the second stage gain, the code

1000 0000 0001 11 00 10 0000 0000 0111 1111 1110

can be used. Since the second stage gain parameter value is only three bits long, the FILT/DIGOUT pin will have a value of 0 when this code is entered, and will remain 0 during four additional pulses at DIGIN. The fifth, sixth and seventh pulse at DIGIN will return the 3-bit value at FILT/DIGOUT, the seventh pulse returning the LSB. An eighth pulse at DIGIN terminates the read mode.

Sense Current

A sense current is sent across each polysilicon fuse to determine whether it has been blown or not. When the voltage across the fuse is less than approximately 1.5V, the fuse is considered not blown and logic 0 is output from the OTP cell. When the voltage across the fuse is greater than approximately 1.5V, the fuse is considered blown and logic 1 is output.

When the AD8555 is manufactured, all fuses have a low resistance. When a sense current is sent through the fuse, a voltage less than 0.1V is developed across the fuse. This is much lower than 1.5V, so a logic 0 is output from the OTP cell. When a fuse is electrically blown, it should have a very high resistance. When the sense current is applied to the blown fuse, the voltage across the fuse should be larger than 1.5V, so logic 1 is output from the OTP cell.

It is theoretically possible (though very unlikely) for a fuse to be incompletely blown during programming, assuming the required conditions are met. In this situation, the fuse could have a medium resistance (neither low nor high), and a voltage of approximately 1.5V could be developed across the fuse. Thus, the OTP cell could sometimes output a logic 0 or a logic 1, depending on temperature, supply voltage and other variables. To detect this undesirable situation, the sense current can be lowered by a factor of 4 using a special code. The voltage developed across the fuse would then change from 1.5V to 0.38V, and the output of the OTP would be a logic 0 instead of the logic 1 expected from a blown fuse. Correctly blown fuses would still output a logic 1. In this way, incorrectly blown fuses can be detected. Another special code would return the sense current to the normal (larger) value. The sense current cannot be permanently programmed to the low value. When the AD8555 is powered up, the sense current defaults to the high value.

The code to use the low sense current is:
1000 0000 0001 00 00 10 XXXX XXX1 0111 1111 1110

The code to use the normal (high) sense current is:
1000 0000 0001 00 00 10 XXXX XXX0 0111 1111 1110

Suggested Programming Procedure

1. Set VDD and VSS to desired values in the application. Use simulation mode to test and determine desired codes for second stage gain, first stage gain, and output offset. The nominal values for these parameters are given by Tables 1 and 2, and Equations (1) and (2); the codes corresponding to these values can be used as a starting point. However, since actual parameter values for given codes will vary from device to device, some fine tuning will be necessary for the best possible accuracy.

   One way to choose these values is to set the output offset to an approximate value (e.g. code 128 for mid-supply) to allow the required gain to be determined. Then, set the second stage gain such that the minimum first stage gain (code 0) gives a lower gain than required, and the maximum first stage gain (code 127) gives a higher gain than required. After choosing the second stage gain, the first stage gain can be chosen to fine tune the total gain. Finally, the output offset can be adjusted to give the desired value. After determining the desired codes for second stage gain, first stage gain, and output offset, the device is ready for permanent programming.

2. Set VSS to 0V and VDD to 5.5V. Use program mode to permanently enter the desired codes for second stage gain, first stage gain, and output offset. Blow the master fuse to allow the AD8555 to read data from the fuses and to prevent further programming.

3. Set VDD and VSS to desired values in the application. Use read mode with low sense current followed by high sense current to verify programmed codes.

4. Measure gain and offset to verify correct functionality.

Suggested Algorithm to Determine Optimal Gain and Offset Codes

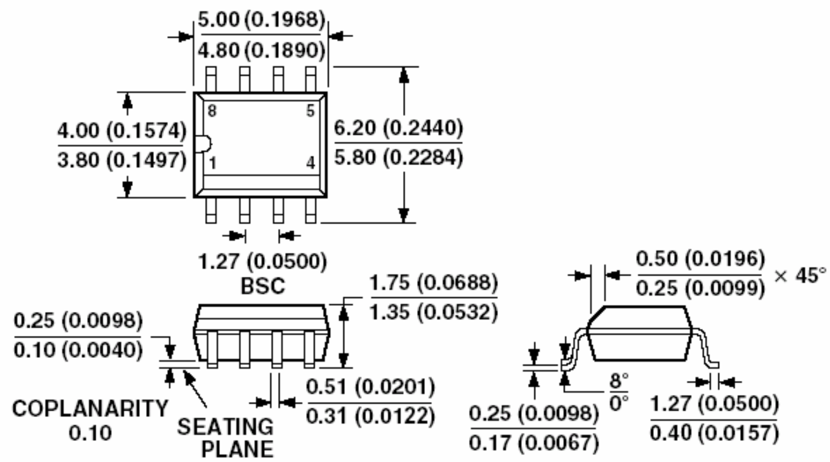
1. Determine desired gain, G_A (e.g. using measurements).

2A. Use Table 2 to determine the second stage gain G_2 such that $(4.00*1.04) < (G_A/G_2) < (6.4/1.04)$. This ensures that the first and last codes for the first stage gain are not used, thereby allowing enough first stage gain codes within each second stage gain range to adjust for the 3% accuracy.
2B. Use simulation mode to set the second stage gain to G_2.

3A. Set the output offset to allow the AD8555 gain to be measured (e.g. use code 128 to set it to mid-supply).
3B. Use Table 1 or Equation (3) to set the first stage gain code C_{G1} such that first stage gain is nominally G_A/G_2.
3C. Measure resulting gain G_B. G_B should be within 3% of G_A.
3D. Calculate first stage gain error (in relative terms) $E_{G1} = G_B/G_A - 1$.
3E. Calculate error (in number of first stage gain codes) $C_{EG1} = E_{G1}/0.00370$.
3F. Set first stage gain code to $C_{G1} - C_{EG1}$.
3G. Measure gain G_C. G_C should be closer to G_A than G_B.
3H. Calculate error (in relative terms) $E_{G2} = G_C/G_A - 1$.
3I. Calculate error (in number of first stage gain codes) $C_{EG2} = E_{G2}/0.00370$.
3J. Set first stage gain code to $C_{G1} - C_{EG1} - C_{EG2}$. The resulting gain should be within one code of G_A.

4A. Determine desired output offset O_A (e.g. using measurements).
4B. Use equation (1) to set output offset code C_{O1} such that output offset is nominally O_A.
4C. Measure output offset O_B. O_B should be within 3% of O_A.
4D. Calculate error (in relative terms) $E_{O1} = O_B/O_A - 1$.
4E. Calculate error (in number of output offset codes) $C_{EO1} = E_{O1}/0.00392$.
4F. Set output offset code to $C_{O1} - C_{EO1}$.
4G. Measure output offset O_C. O_C should be closer to O_A than O_B.
4H. Calculate error (in relative terms) $E_{O2} = O_C/O_A - 1$.
4I. Calculate error (in number of output offset codes) $C_{EO2} = E_{O2}/0.00392$.
4J. Set output offset code to $C_{O1} - C_{EO1} - C_{EO2}$. The resulting offset should be within one code of O_A.

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



16-Lead Lead Frame Chip Scale Package [LFCSP]
4 x 4 mm Body
(CP-16)
Dimensions shown in millimeters